VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DELAY CELLS

This application claims the benefit of U.S. provisional patent application No. 60/323,249, filed
5 September 18, 2001, which is hereby incorporated by reference herein in its entirety.

Background of the Invention

This invention relates to voltage controlled oscillator ("VCO") circuits, and more particularly to
10 voltage controlled oscillator circuits that can be programmed to operate in any of several frequency ranges over a very wide band of such frequency ranges.

Phase locked loop ("PLL") circuitry is frequently used for such purposes as helping to
15 retrieve data from a signal that may vary in frequency and/or phase. The PLL may be in relatively general-purpose circuitry such as a programmable logic device ("PLD") that may need to support signaling at any frequency in a wide range of frequencies. (For
20 examples of PLDs employing PLLs, see Aung et al. U.S. patent application No. 09/805,843, filed March 13, 2001.) The range of frequencies over which a PLL may be required to operate is steadily increasing, particularly at the upper end (i.e., higher
25 frequencies). At the same time, power supply voltages

for integrated circuits are decreasing, making it more difficult to extend the operating range of PLL circuits.

Summary of the Invention

5   A delay cell (e.g., for use in the voltage controlled oscillator ("VCO") of a PLL) includes a plurality of load resistance transistors connectable in parallel with one another, a plurality of bias current transistors connectable in parallel with one another,

10   and a switching transistor connected in series between the load resistance transistors and the bias current transistors. Switching circuitry allows the number of the load resistance transistors that are actually operating in parallel to be selected. Other switching

15   circuitry similarly allows the number of the bias current transistors that are actually operating in parallel to be similarly selected. This ability to essentially reconfigure the delay cell allows the operating range (i.e., the time delay characteristic)

20   of the delay cell to be greatly extended. A VCO may include a plurality of such delay cells connected in a closed loop series. The extended operating range of the delay cells similarly greatly extends the operating frequency range of a VCO made up of such cells. The

25   same is true for the operating range of a PLL that includes such a VCO.

The delay cell may be differential in construction and operation.

Further features of the invention, its nature

30   and various advantages will be more apparent from the accompanying drawings and the following detailed description.

Brief Description of the Drawings

FIG. 1 is a simplified schematic block diagram of an illustrative, conventional, phase locked loop ("PLL") circuit.

5   FIG. 2 is a simplified schematic block diagram of an illustrative, conventional, voltage controlled oscillator ("VCO") circuit.

FIG. 3 is a simplified schematic diagram of an illustrative, conventional differential delay cell

10   circuit.

FIG. 4 is a simplified schematic block diagram of an illustrative programmable differential delay cell circuit in accordance with the invention.

FIG. 5 is a simplified schematic block

15   diagram of an alternative embodiment of a representative portion of what is shown in FIG. 4.

FIG. 6A is a simplified, illustrative, circuit performance diagram useful in explaining certain aspects of the invention.

20   FIG. 6B is similar to FIG. 6A but illustrates the extended range of operation achievable in accordance with the invention.

FIG. 7A and 7B are respectively similar to FIGS. 6A and 6B for other aspects of the invention.

25   FIG. 8 is a simplified schematic block diagram of an illustrative system employing a PLD that includes PLL circuitry having a VCO that employs delay cells in accordance with the invention.

Detailed Description

In the illustrative, conventional, PLL circuit 10 shown in FIG. 1, phase/frequency detector ("PFD") circuit 20 receives an input signal via input lead 8. Signal 8 is a time-varying signal such as a binary digital signal conveying data represented by different voltage levels and/or by voltage level transitions. PFD 20 compares the phase and frequency of signal 8 to the phase and frequency of a signal fed back to PFD 20 from VCO 30 via lead 32. Based on that comparison, PFD 20 produces one or more output signals 22 for controlling VCO 30 to make the phase and frequency of signal 32 more closely match the phase and frequency of signal 8. For example, signal 8 may be a CDR (clock data recovery) data signal, and PLL 10 may be operated to provide a clock signal recovered from the CDR data signal. (The recovered clock signal can be signal 32 or a signal synchronized with but shifted in phase relative to signal 32, depending on the application.) If PFD 20 detects that signal 32 is too low in frequency or is delayed in phase relative to signal 8, PFD 20 produces an output signal or signals 22 for increasing the frequency of VCO 30. Alternatively, if PFD 20 detects that signal 32 is too high in frequency or is advanced in phase relative to signal 8, PFD 20 produces an output signal or signals 22 for decreasing the frequency of VCO 30.

An illustrative construction of VCO 30 is shown in FIG. 2. In this embodiment VCO 30 includes a plurality of differential delay cells 40 connected in a closed loop series. Each delay cell 40 produces transitions in its differential output signals a time delay interval after receiving transitions in the

differential signals applied to it from the preceding
delay cell in the closed loop series. The time delay
interval of each delay cell 40 is variable to at least
some degree, with the variation being controlled by the
5   output signal(s) 22 of PFD 20 (FIG. 1). The frequency
of oscillation of VCO 30 is inversely proportional to
the time delay of delay cells 40. In order for PLL 10
to be able to lock onto any frequency in a wide range
of frequencies, VCO 30 must have a correspondingly wide
10   range of oscillation frequencies. This means that
delay cells 40 must have a wide range of possible delay
time intervals.

An illustrative construction of one
representative delay cell 40 is shown in more detail in
15   FIG. 3. Although FIG. 3 shows a delay cell with
PMOSFETs as load resistors RL1 and RL2, and NMOSFETs as
input transistors SW1/SW2 and current mirror circuitry
IBIAS, it will be understood that similar operation can
be achieved with NMOSFETs as load resistors and with
20   PMOSFETs as input transistors and current mirror
circuitry.

In the circuitry shown in FIG. 1 RCONT and
VCONT are control signals from PFD 20 (FIG. 1).
Signals VIN- and VIN+ are differential input signals
25   from the preceding delay cell 40 in the closed loop
series (see FIG. 2). Signals VO- and VO+ are
differential output signals to the next delay cell 40
in the closed loop series (see again FIG. 2).

The time delay of delay cell 40 is
30   proportional to the resistance of load resistors RL1
and RL2. Therefore, to achieve a wide frequency range,
load resistors RL1 and RL2 are varied with RCONT and
have a wide resistance range. Also the tail current

IBIAS is controlled with VCONT and has a wide current range. The tail current IBIAS is responsible for keeping the output voltage swing constant as load resistance changes. Traditionally, to increase

5 frequency, RCONT is decreased, which increases gate-source bias voltage, thus decreasing resistances RL1 and RL2. At the same time, VCONT is increased, which increases gate-source bias voltage, thus increasing tail current IBIAS. At maximum RL1 and RL2, the load

10 resistance control voltage RCONT starts at VDD - (VSW + |VTP|) and can be decreased until approximately VSS + VDS (assuming that basic current mirroring is used for biasing), at which point RL1 and RL2 are at minimum. VSW is the maximum swing voltage, or VDD - VO, when VO

15 is at its minimum. Current mirror control voltage VCONT starts at VGS, required for minimum current, and can be increased until approximately VDD - VSD (assuming that basic current mirroring is used for biasing), at which point IBIAS is at its maximum.

20   For both control voltages (i.e., for both RCONT and VCONT) power supply VDD becomes the limiting factor for increasing frequency. Higher bandwidth can be achieved with higher power supply. Unfortunately, the power supply for future integrated circuits is

25 shrinking. This creates a requirement for a different design approach.

        In multi-function integrated circuits such as PLDs it is necessary to design PLLs for various high-speed I/O standards with wideband frequency operation.

30 However, as the power supply shrinks, this becomes extremely challenging. The concept of a programmable delay cell in accordance with this invention (see, for example, FIG. 4) solves the need to meet wideband

frequency operation in multi-function integrated
circuits for such purposes as high-speed communication
applications.

The illustrative programmable delay cell 40'
5   in accordance with this invention that is shown in
FIG. 4 operates on the same principles as the
traditional delay cell, with the addition of an option
to turn on a selectable number of extra transistors in
parallel with the default devices. For example, load
10 resistor RL1 in FIG. 3 is replaced in FIG. 4 by a
plurality of load resistors RL1a, RL1b, ..., RL1n
connected (from source to drain) in parallel with one
another. Similarly, load resistor RL2 is replaced by a
plurality of load resistors RL2a, RL2b, ..., RL2n
15 connected (from source to drain) in parallel with one
another. The IBIAS transistor ICONT is similarly
replaced by a plurality of transistors ICONTa, ICONTb,
..., ICONTn connected (from source to drain) in
parallel with one another. In each case the "a"
20 transistor (i.e., RL1a, RL2a, and ICONTa) is the
default device or transistor.

Each transistor (other than the default
transistor) in each group of parallel transistors is
activated/deactivated via a multiplexer that is
25 controlled by other associated circuitry. For example,
RL1b and RL2b are controlled in tandem by the output
signal of multiplexer 110b. This multiplexer is
controllable to output either VDD (which turns off
transistors RL1b and RL2b) or RCONT (which gives RL1b
30 and RL2b exactly the same control as RL1a and RL2a).
the latter condition of multiplexer 110b causes RL1a
and RL1b to operate in parallel with one another, and
similarly causes RL2a and RL2b to operate in parallel

with one another. Other multiplexers in the group
110b-110n operate similarly to allow other transistors
in the groups RL1b-RL1n and RL2b-RL2n to be selectively
added into parallel operation with default transistors
5 RL1a and RL2a.

Multiplexers 120b-120n similarly allow any
selectable number of additional transistors ICONTb-
ICONTn to be added into parallel operation with default
transistor ICONTa. For example, multiplexer 120b is
10 controllable to apply either VSS or VCONT to the gate
of transistor ICONTb. Applying VSS deactivates
transistor ICONTb. On the other hand, applying VCONT
gives transistor ICONTb the same operation as
transistor ICONTa.

15 In the illustrative embodiment shown in
FIG. 4, each multiplexer 110/120 is programmably
controlled by an associated programmable memory cell
112/122. For example, multiplexer 110b is controlled
to output either VDD or RCONT by the programmed state
20 of memory cell 112b. Memory cells like 112/122 are
sometimes alternatively referred to herein as function
control elements ("FCEs").

As an alternative to programmable (and
therefore typically relatively static) control of
25 multiplexers 110/120, those devices can instead be
controlled by other types of signals that can be more
dynamic. For example, such more dynamic control
signals may come from PFD 20 (FIG. 1) or from logic
circuitry elsewhere on a PLD that includes the
30 circuitry of this invention. FIG. 5 shows illustrative
circuitry for allowing control of a representative
multiplexer 110/120 to be controlled either statically
or dynamically. In FIG. 5 multiplexer 110/120 is

controlled by the output signal of multiplexer 130.
Multiplexer 130 is controlled by the output signal of
FCE 132 to output either of the two other input signals
that it receives. These two other input signals are a

5   so-called dynamic control signal and the output signal
of FCE 134. If multiplexer 130 routes the output
signal of FCE 134 to multiplexer 110/120, then
multiplexer 110/120 can be controlled to always output
either one or the other of its two non-control inputs

10   depending on the programmed state of FCE 134. On the
other hand, if multiplexer 130 is controlled by FCE 132
to route the dynamic control signal to multiplexer
110/120, multiplexer 110/120 can be controlled to
output one or the other of its two non-control inputs

15   at different times depending on the current logical
state of the dynamic control signal.

Circuit elements like 110, 120, and 130 are
sometimes referred to herein as programmable logic
connectors ("PLCs"), and this PLC terminology may be

20   used without regard for whether the circuitry referred
to is programmably or dynamically controlled.

Returning to FIG. 4, all ranges of operation
of illustrative programmable differential delay
cell 40' (i.e., ranges a-n) have the same operating

25   limits on RCONT and VCONT as the traditional delay·
cell. Nevertheless, much higher frequency can be
achieved by turning on optional devices (ranges b-n).
This is due to the reduced load resistance, which
reduces delay cell time constant as described

30   previously. Extra transistors in the current mirror
provide more total tail current IBIAS, which maintains
the output swing, while extra load transistors add more
resistors in parallel to reduce the load resistance.

In the programmable delay cell the load resistance RL
becomes a parallel combination of multiple load
resistors according to the equation $1/RL = 1/RLa + 1/RLb + ... + 1/RLn$. When all resistors are equal with
5   a value of R, then the total resistance is simply R/n,
which shows that the load resistance will decrease as
more optional transistors are activated. If all
resistors are not equal, then the total resistance of
an arbitrary number of resistors in parallel is always
10   less than the smallest resistor in the combination.

FIGS. 6A and 7A illustrate the relatively
limited operating range of a traditional delay cell of
the type shown in FIG. 3. FIG. 6A shows that in the
traditional load cell the attainable load resistance
15   range is limited by the power supply. Similarly,
FIG. 7A shows that in the traditional load cell the
tail current range is limited by the power supply. In
contrast, FIGS. 6B and 7B illustrate the much greater
operating range of the programmable delay cell of this
20   invention (e.g., as in FIG. 4). FIG. 6B shows that in
the programmable delay cell (e.g., 40') the attainable
load resistance range is limited substantially only by
the number of transistors in parallel that are provided
by the designer. FIG. 7B illustrates the same point
25   for the attainable tail current range in a programmable
delay cell like 40'.

To briefly recapitulate some of the points
made above, the operating range needed in a dynamic VCO
differential delay cell is a direct product of
30   constantly expanding features of devices such as PLDs
(e.g., the need of such devices to operate in multiple,
high-speed-serial communications standards). To
incorporate standards such as Gigabit Ethernet,

Infiniband, and Xaui with older SONET standards, high-speed PLLs have to expand in operating bandwidth from a couple of hundred megahertz to 1-2 GHz. Couple that with the ongoing reduction in integrated circuit power

5   supply, and it becomes difficult or impossible to design wideband PLLs in a traditional manner. The new programmable approach shown and described herein offers a solution that may be especially useful to manufacturers of PLDs. The bandwidth of the PLL

10   including programmable VCO delay cells can be expanded until it encounters physical process limits. However, within these process limits bandwidth is not limited by the power supply, but rather by the design engineer.

        FIG. 8 shows a programmable logic device

15   ("PLD") 14 (including PLL 10 and programmable logic 12) in a data processing system 202. PLL 10 may be like PLL 10 in FIG. 1, except that it includes in its VCO 30 delay cells constructed in accordance with this invention (e.g., delay cells 40' as shown in FIG. 4).

20   Programmable logic 12 may be conventional and may make use of signal(s) output by PLL 10 and/or may produce signals for controlling certain aspects of the operation of PLL 10 (e.g., controlling PLCs 110 and/or 120 in FIG. 4). Data processing system 202 may also

25   include one or more of the following components: a processor 204; memory 206; I/O circuitry 208; and peripheral devices 210. These components are coupled together by a system bus 220 and are populated on a circuit board 230 that is contained in an end-user

30   system 240.

        System 202 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital

signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. Programmable logic device 14 can be used to perform a variety of different logic functions. For

5 example, programmable logic device 14 can be configured as a processor or controller that works in cooperation with processor 204. Programmable logic device 14 may also be used as an arbiter for arbitrating access to a shared resource in system 202. In yet another example,

10 programmable logic device 14 can be configured as an interface between processor 204 and one of the other components in system 202. It should be noted that system 202 is only exemplary, and that the true scope and spirit of the invention should be indicated by the

15 following claims.

Various technologies can be used to implement programmable logic devices 14 in accordance with this invention, as well as the various components of those devices (e.g., the above-described PLL and programmable

20 logic circuitries 10 and 12 and circuit elements like PLCs and FCEs that may be used therein). For example, each PLC can be a relatively simple programmable connector such as a switch or a plurality of switches for connecting any one of several inputs to an output.

25 Alternatively, each PLC can be a somewhat more complex element that is capable of performing logic (e.g., by logically combining several of its inputs) as well as making a connection. In the latter case, for example, each PLC can be product term logic, implementing

30 functions such as AND, NAND, OR, or NOR. Examples of components suitable for implementing PLCs are EPROMs, EEPROMs, pass transistors, transmission gates, antifuses, laser fuses, metal optional links, etc. As

has been mentioned, the various components of PLCs can
be controlled by various, programmable, function
control elements ("FCEs"). (With certain PLC
implementations (e.g., fuses and metal optional links)

5   separate FCE devices are not required.) FCEs can also
be implemented in any of several different ways. For
example, FCEs can be SRAMs, DRAMs, first-in first-out
("FIFO") memories, EPROMs, EEPROMs, function control
registers (e.g., as in Wahlstrom U.S. patent

10 3,473,160), ferro-electric memories, fuses, antifuses,
or the like. From the various examples mentioned above
it will be seen that this invention is applicable to
both one-time-only programmable and reprogrammable
devices.

15   It will be understood that the foregoing is
only illustrative of the principles of the invention,
and that various modifications can be made by those
skilled in the art without departing from the scope and
spirit of the invention. For example, although FIG. 4

20 at least pictorially implies that the sources of the
control signals for PLCs 100, on the one hand, and PLCs
120, on the other hand, are separate, common or shared
control may be used if desired. Such common or shared
control would typically mean that the same control

25 would be used for PLCs 110b and 120b, that the same
control would be used for PLCs 110c and 120c, etc. As
another example of modifications within the scope of
the invention, any number of parallel transistors can
be included in each group RL1a-n, RL2a-n, and ICONTa-n.

30 Although differential delay cells are generally
preferred, the invention can also be applied to non-
differential delay cells. For example, such a non-
differential delay cell would have only one switching

transistor SW1 or SW2, and only one set of load
resistor transistors RL1a-n or RL2a-n.   In other
respects, such a non-differential delay cell can be
constructed as shown, for example, in FIG. 4.